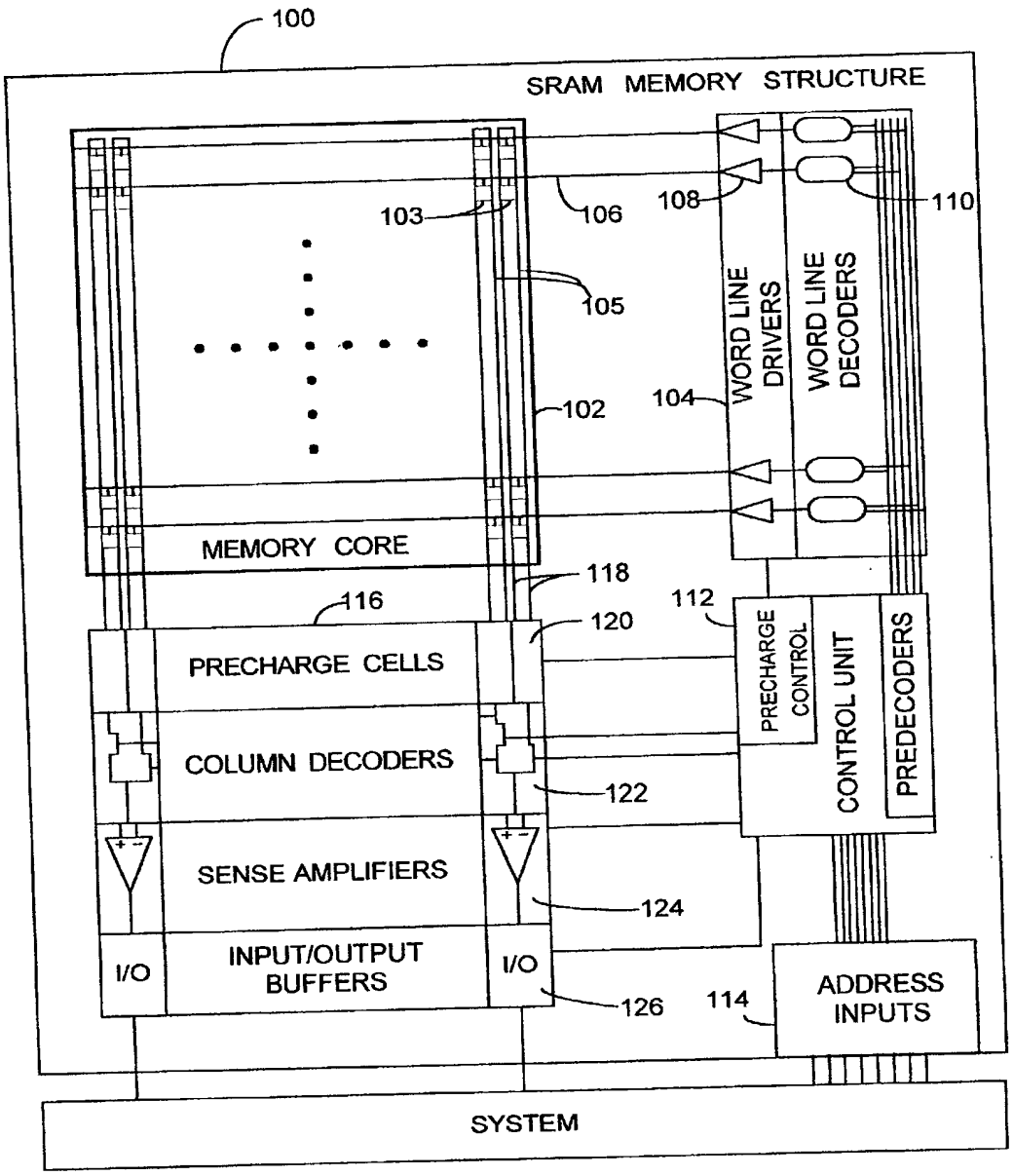
100
SRAM MEMORY STRUCTURE
103
106
108
110
105
WORD LINE DRIVERS
WORD LINE DECODERS
102
104
MEMORY CORE
118
116
112
120
PRECHARGE CELLS
PRECHARGE CONTROL
CONTROL UNIT
PREDECODERS
COLUMN DECODERS
122
SENSE AMPLIFIERS
124
I/O
INPUT/OUTPUT BUFFERS
I/O
126
114
ADDRESS INPUTS
SYSTEM

FIG. 1

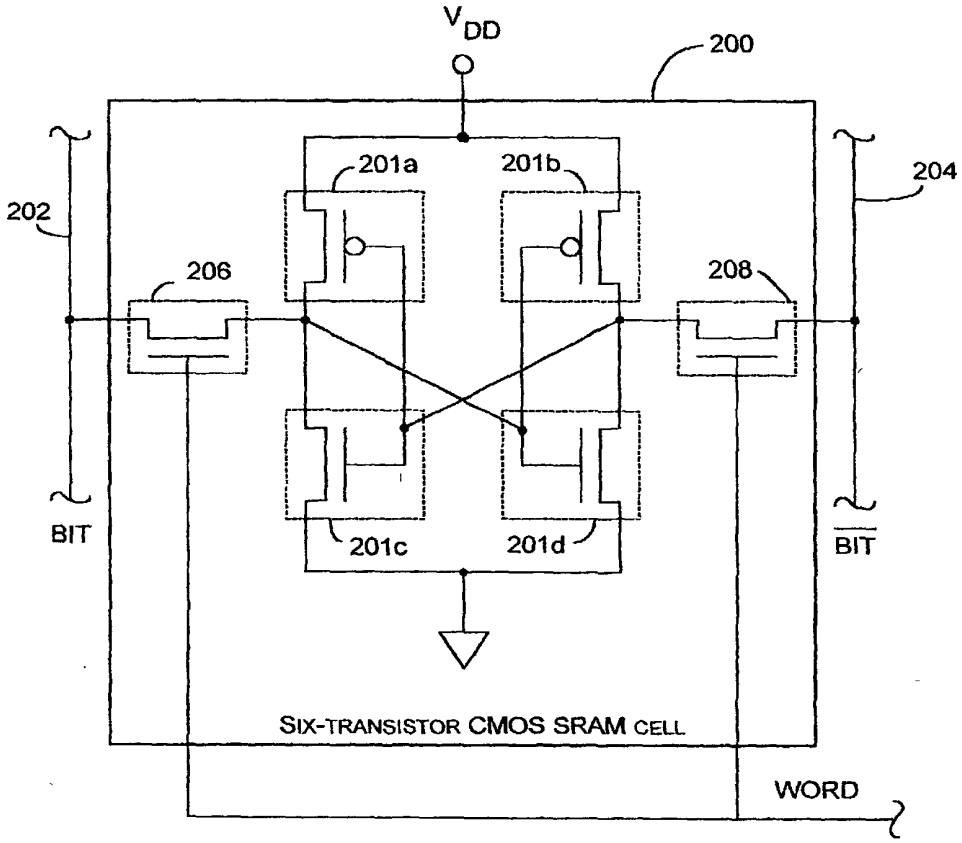
V_{DD}
200
201a
201b
202
204
206
208
BIT
$\overline{BIT}$
201c
201d
SIX-TRANSISTOR CMOS SRAM CELL
WORD

FIG. 2

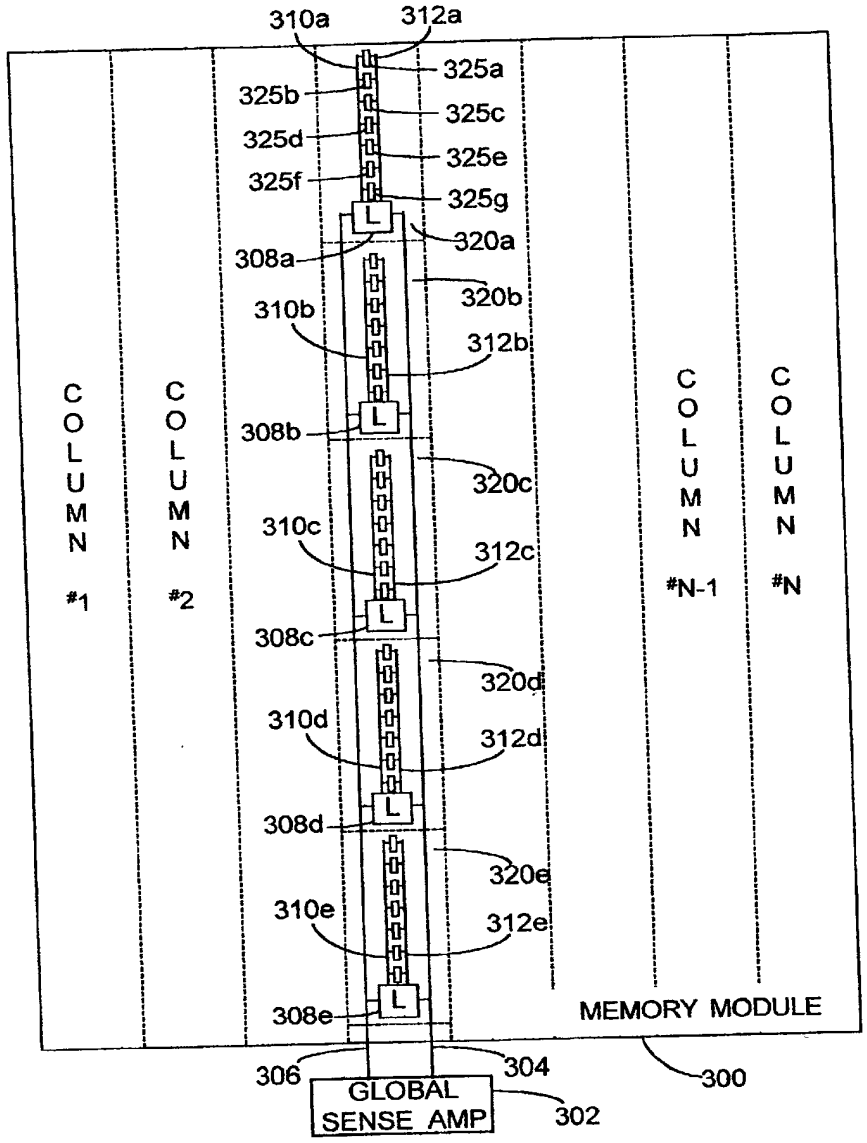
310a
312a
325a
325b
325c
325d
325e
325f
325g
320a
308a
320b
310b
312b
308b
320c
310c
312c
308c
320d
310d
312d
308d
320e
310e
312e
308e
COLUMN #1
COLUMN #2
COLUMN #N-1
COLUMN #N
MEMORY MODULE
306
304
GLOBAL SENSE AMP
302
300

FIG. 3

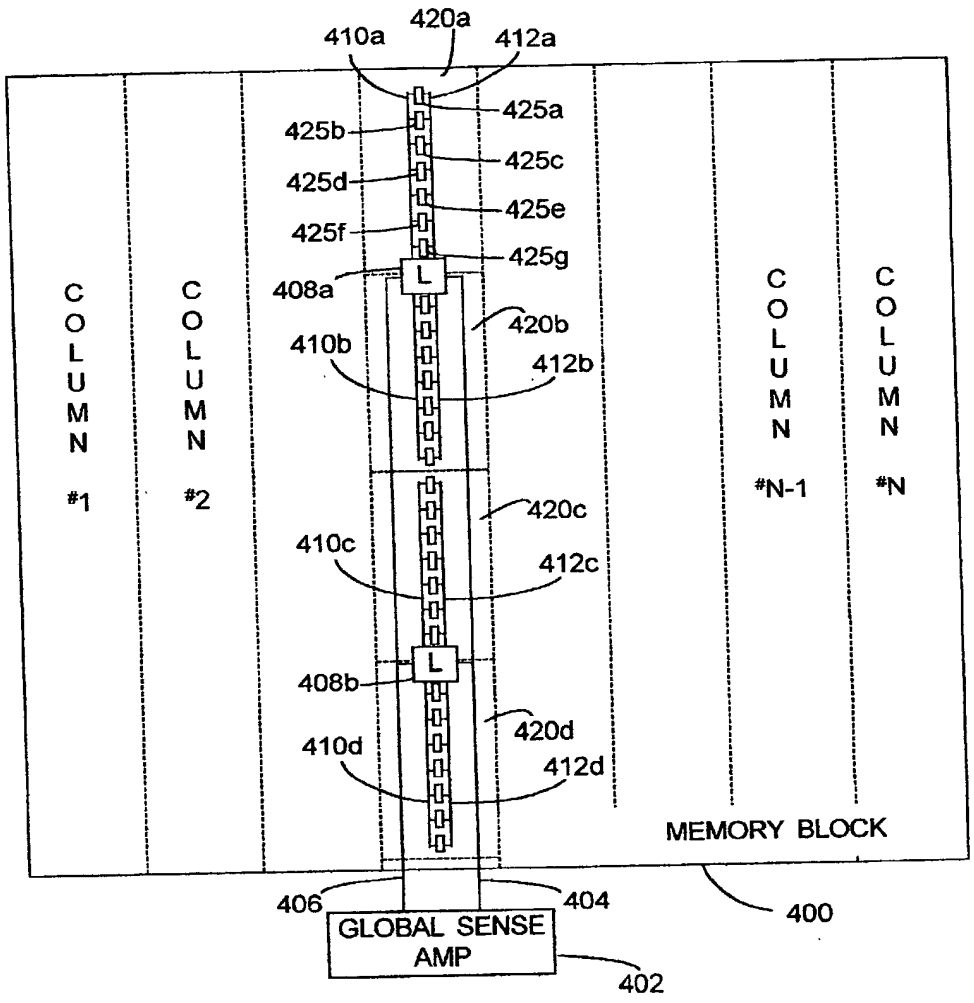
420a
410a
412a
425a
425b
425c
425d
425e
425f
425g
408a
L
420b
410b
412b
COLUMN #1
COLUMN #2
COLUMN #N-1
COLUMN #N
420c
410c
412c
L
408b
420d
410d
412d
MEMORY BLOCK
406
404
GLOBAL SENSE AMP
400
402

FIG. 4

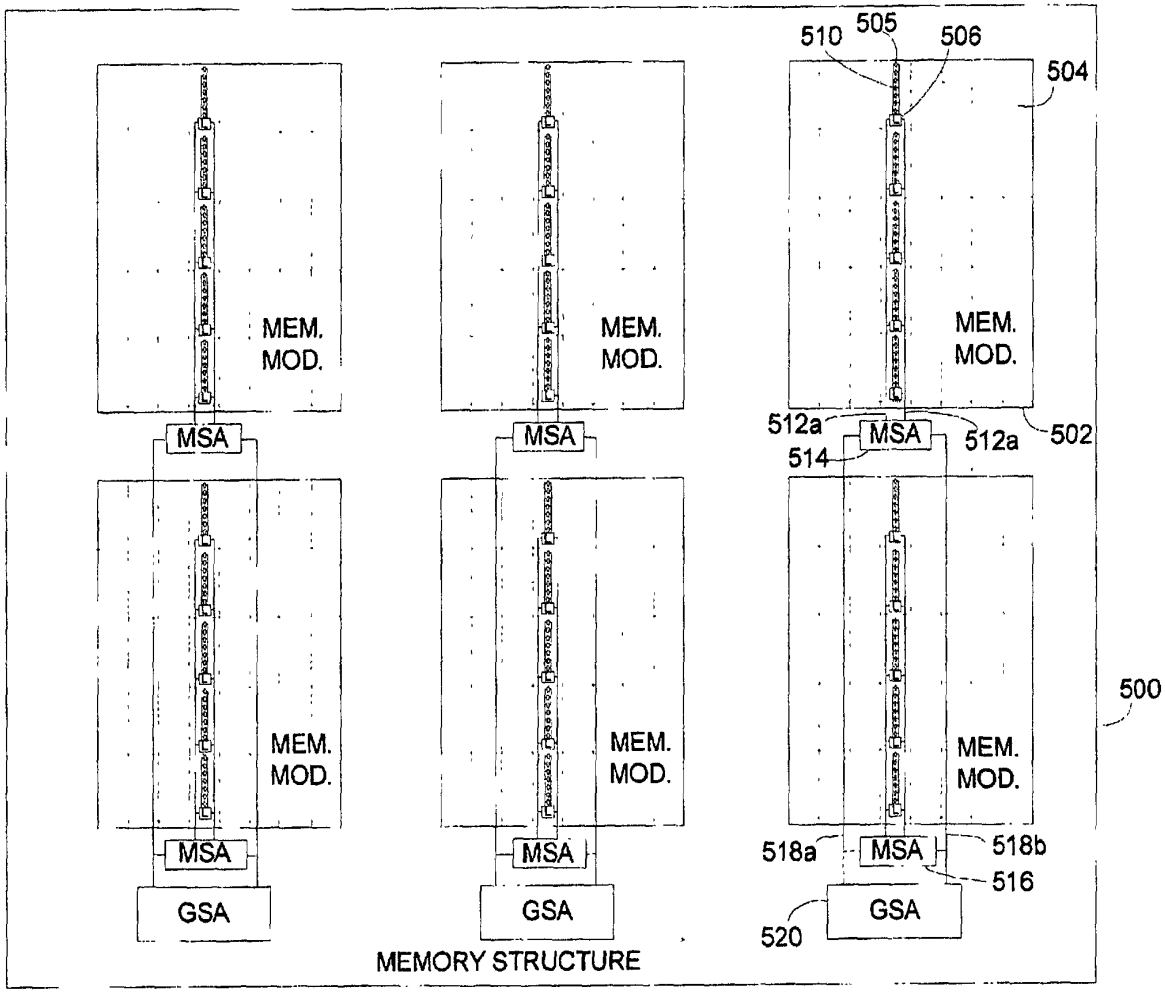
510
505
506
504
MEM. MOD.
MEM. MOD.
MEM. MOD.
512a
MSA
512a
502
514
MSA
MSA
MSA
MEM. MOD.
MEM. MOD.
MEM. MOD.
500
518a
MSA
518b
516
GSA
GSA
GSA
520
MEMORY STRUCTURE

FIG. 5

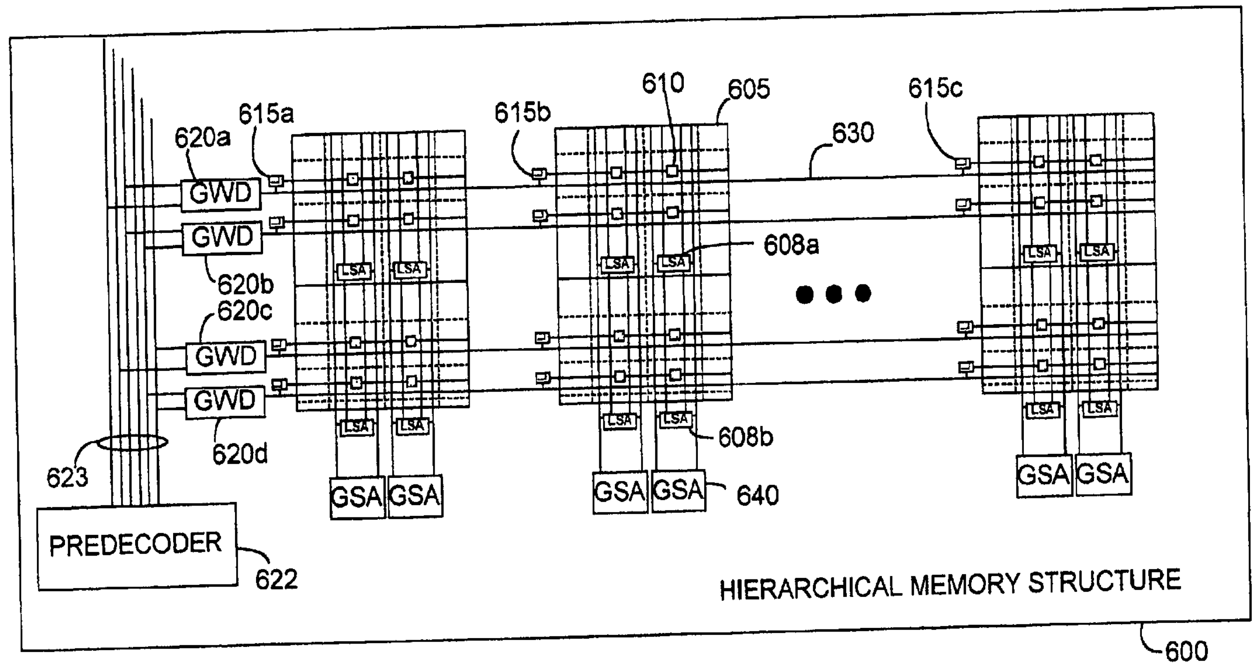
615a
620a
GWD
GWD
620b
620c
GWD
GWD
620d
623
PREDECODER
622
LSA
GSA
GSA
615b
610
605
608a
608b
GSA
GSA
640
630
615c
GSA
GSA
HIERARCHICAL MEMORY STRUCTURE
600

FIG. 6

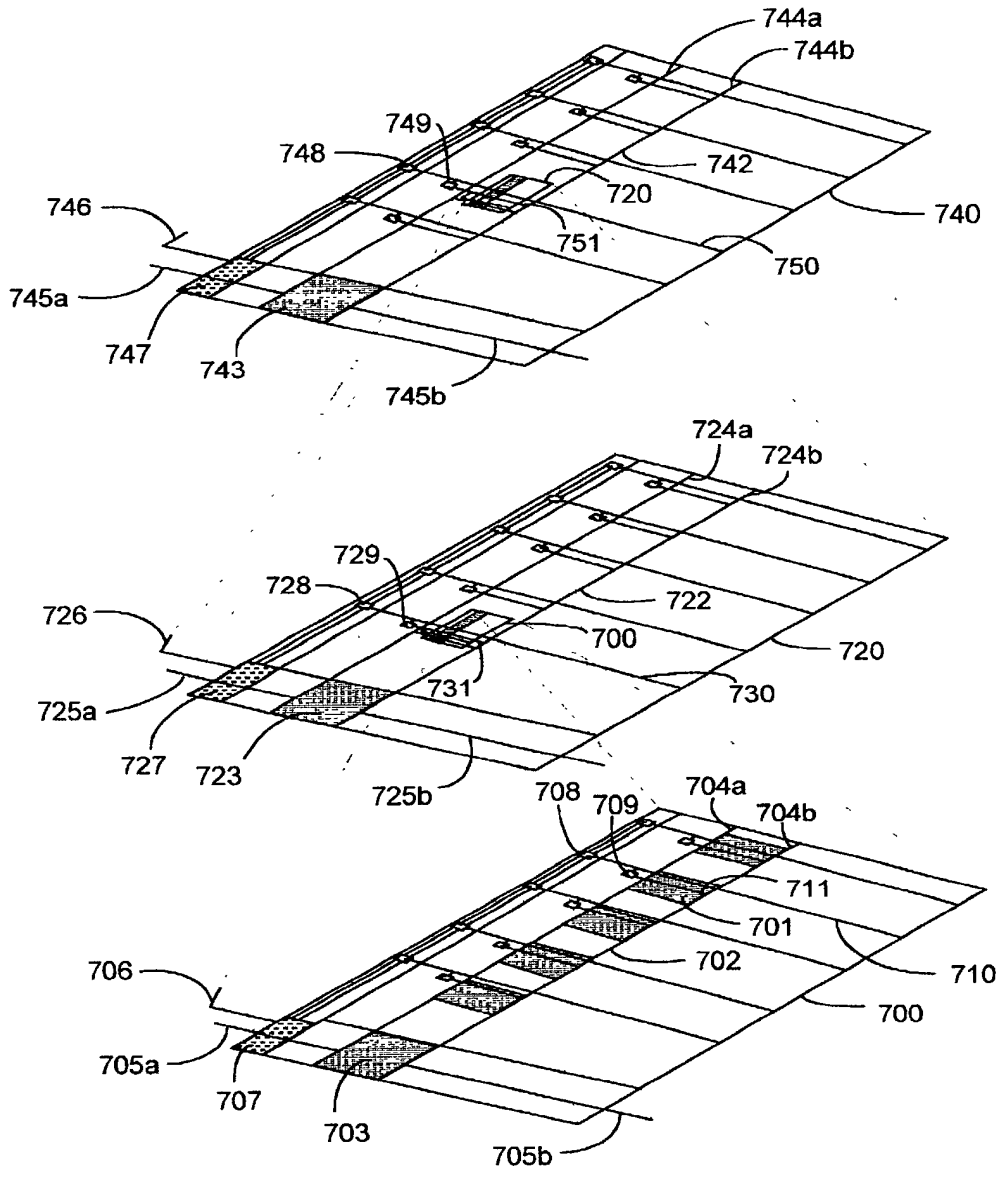
744a
744b
749
748
742
720
746
740
751
750
745a
747
743
745b
724a
724b
729
728
722
726
700
720
731
730
725a
727
723
725b
708
709
704a
704b
711
701
702
706
710
700
705a
707
703
705b

FIG. 7

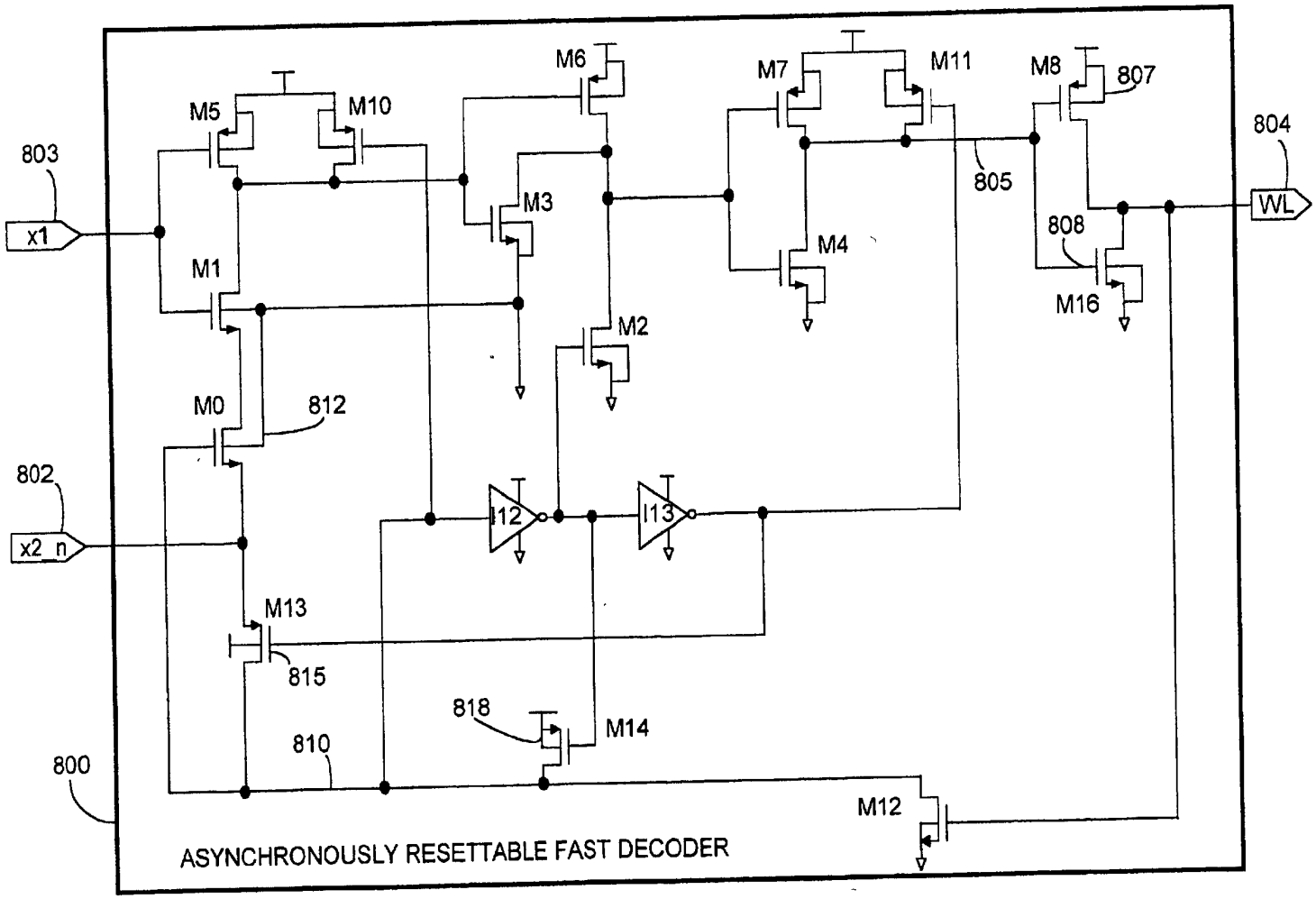

FIG. 8

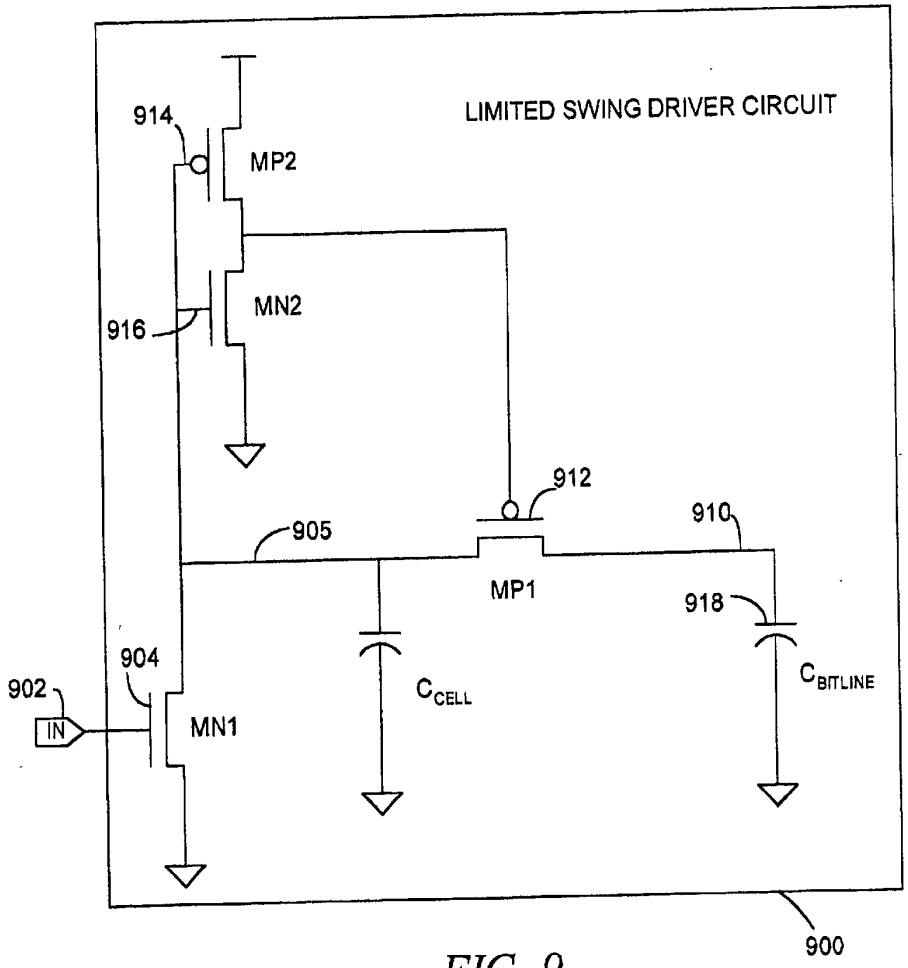

FIG. 9

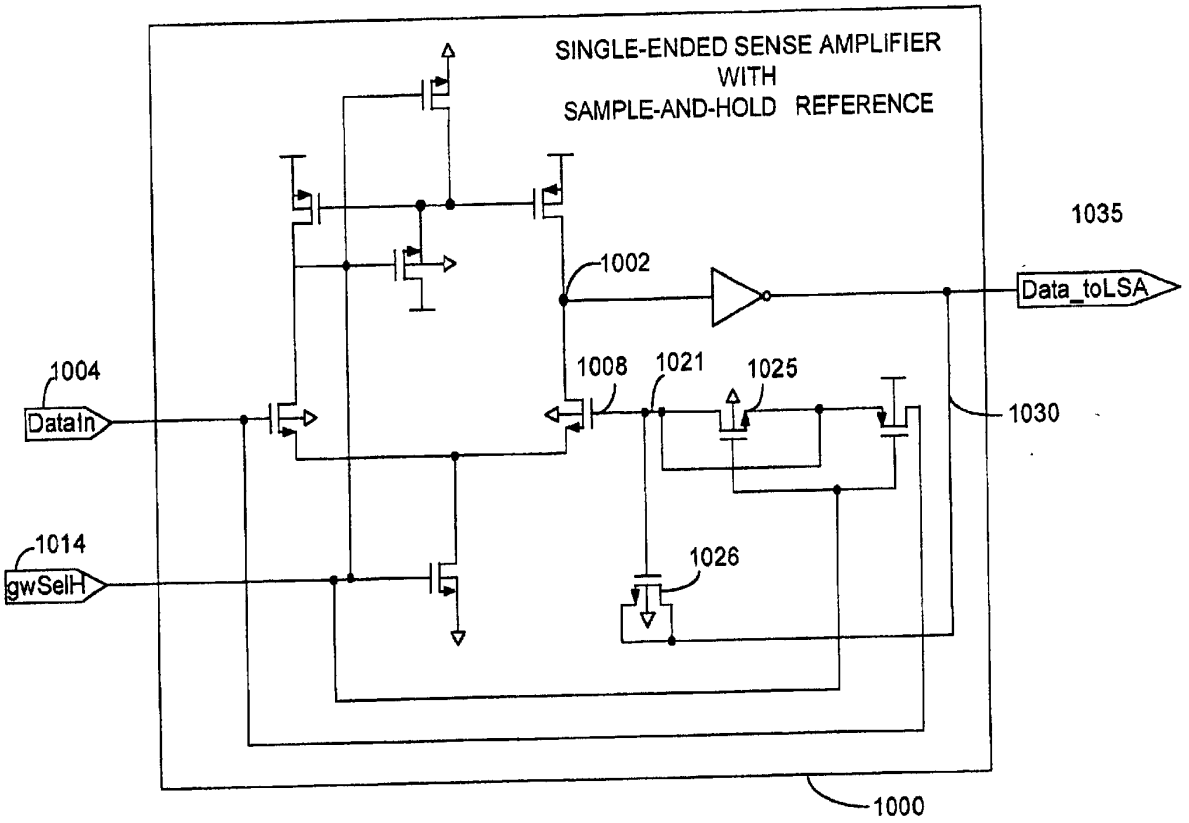
SINGLE-ENDED SENSE AMPLIFIER
WITH
SAMPLE-AND-HOLD REFERENCE
1035
1002
Data_toLSA
1004
DataIn
1008
1021
1025
1030
1014
gwSelH
1026
1000

FIG. 10

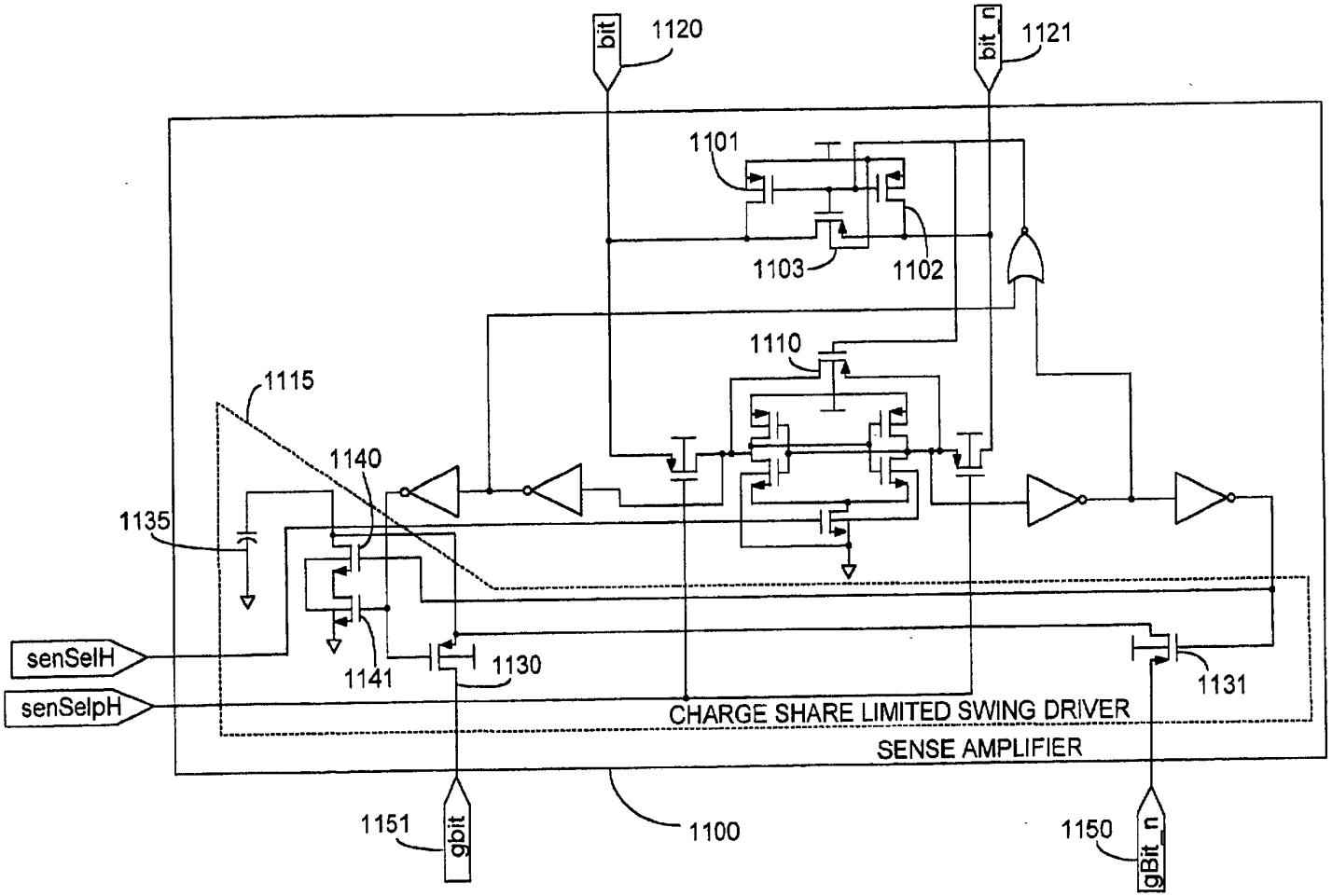

FIG. 11

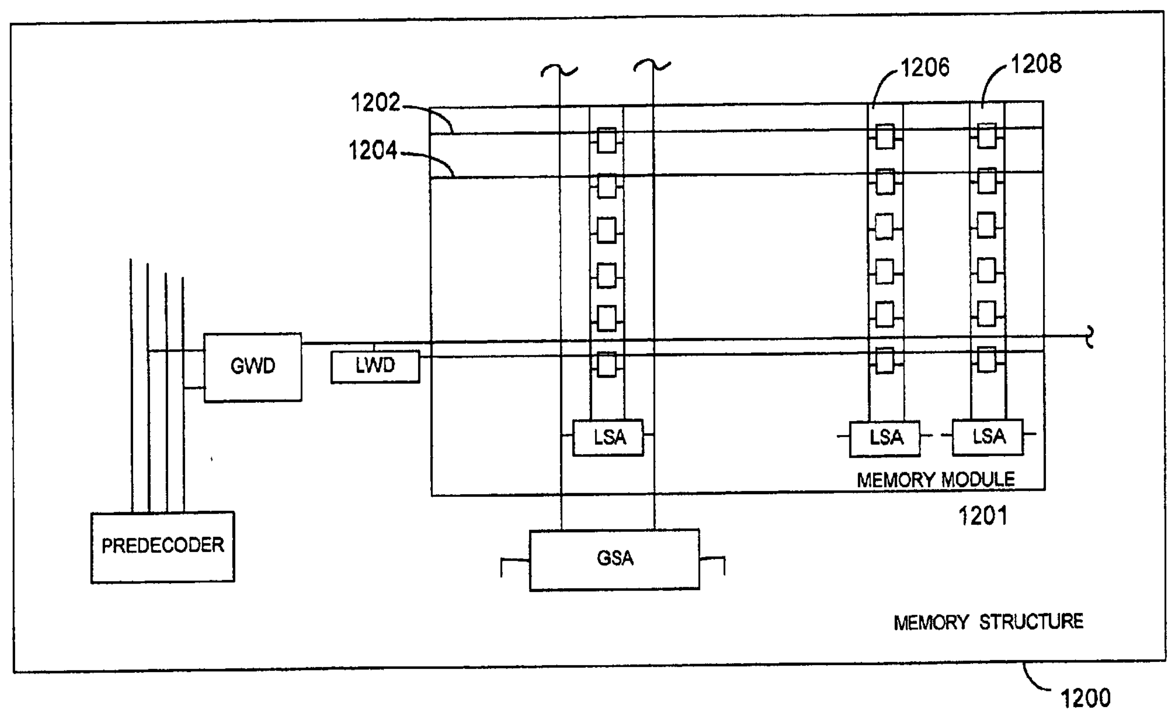

FIG. 12

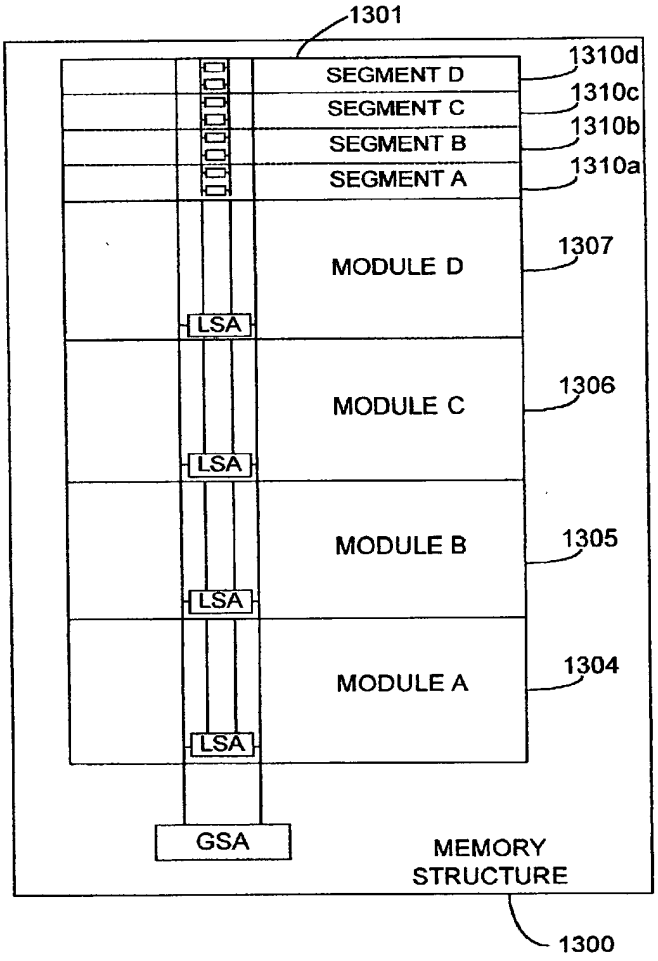
1301
SEGMENT D
SEGMENT C
SEGMENT B
SEGMENT A
1310d
1310c
1310b
1310a
MODULE D
1307
LSA
MODULE C
1306
LSA
MODULE B
1305
LSA
MODULE A
1304
LSA
GSA
MEMORY
STRUCTURE
1300

FIG. 13

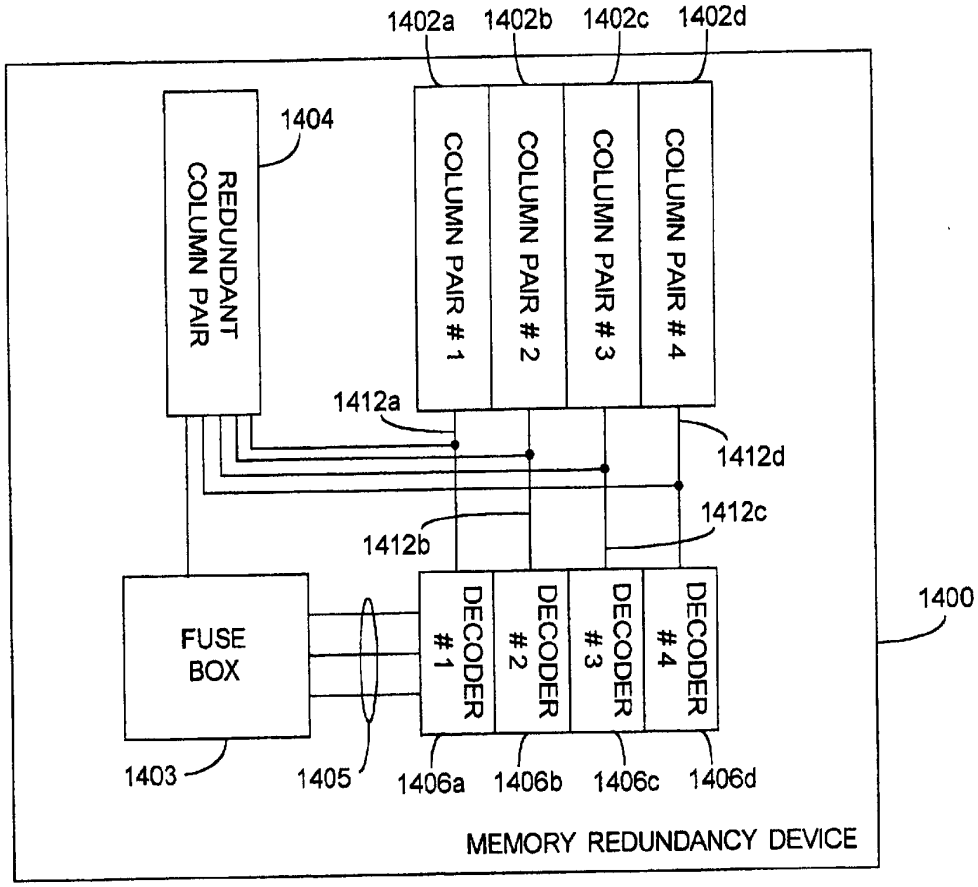

FIG. 14

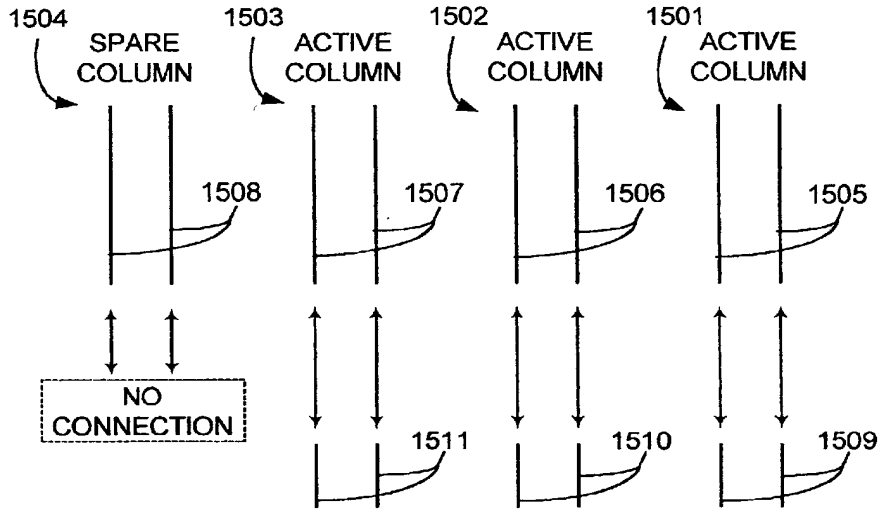

FIG. 15A

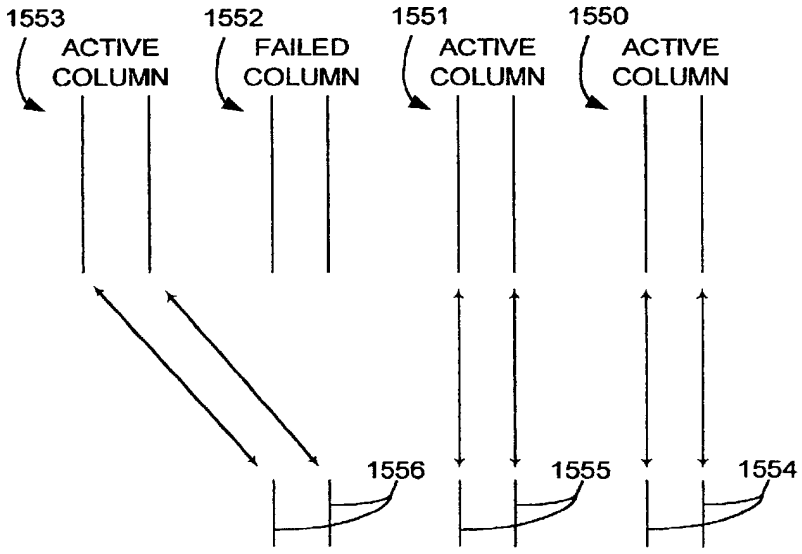

FIG. 15B

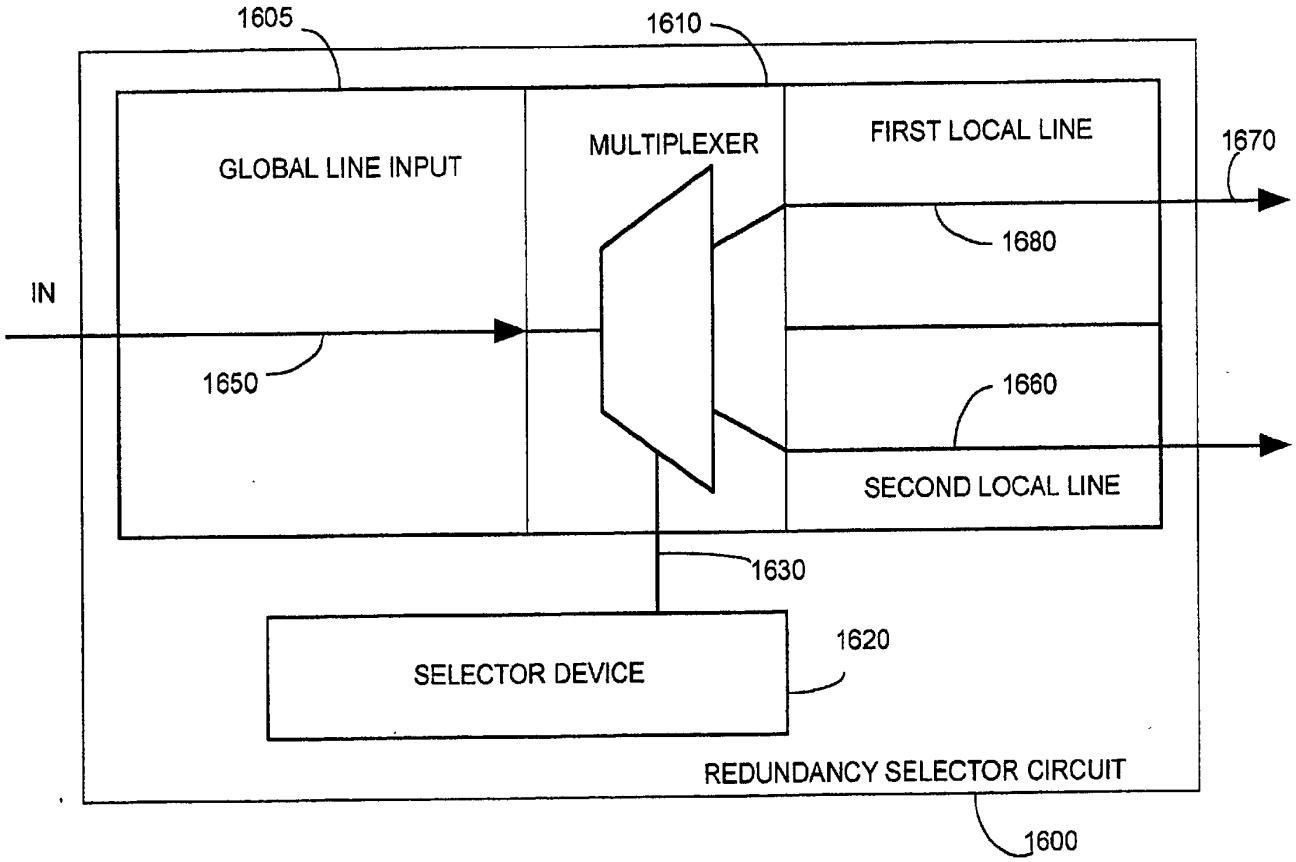

FIG. 16

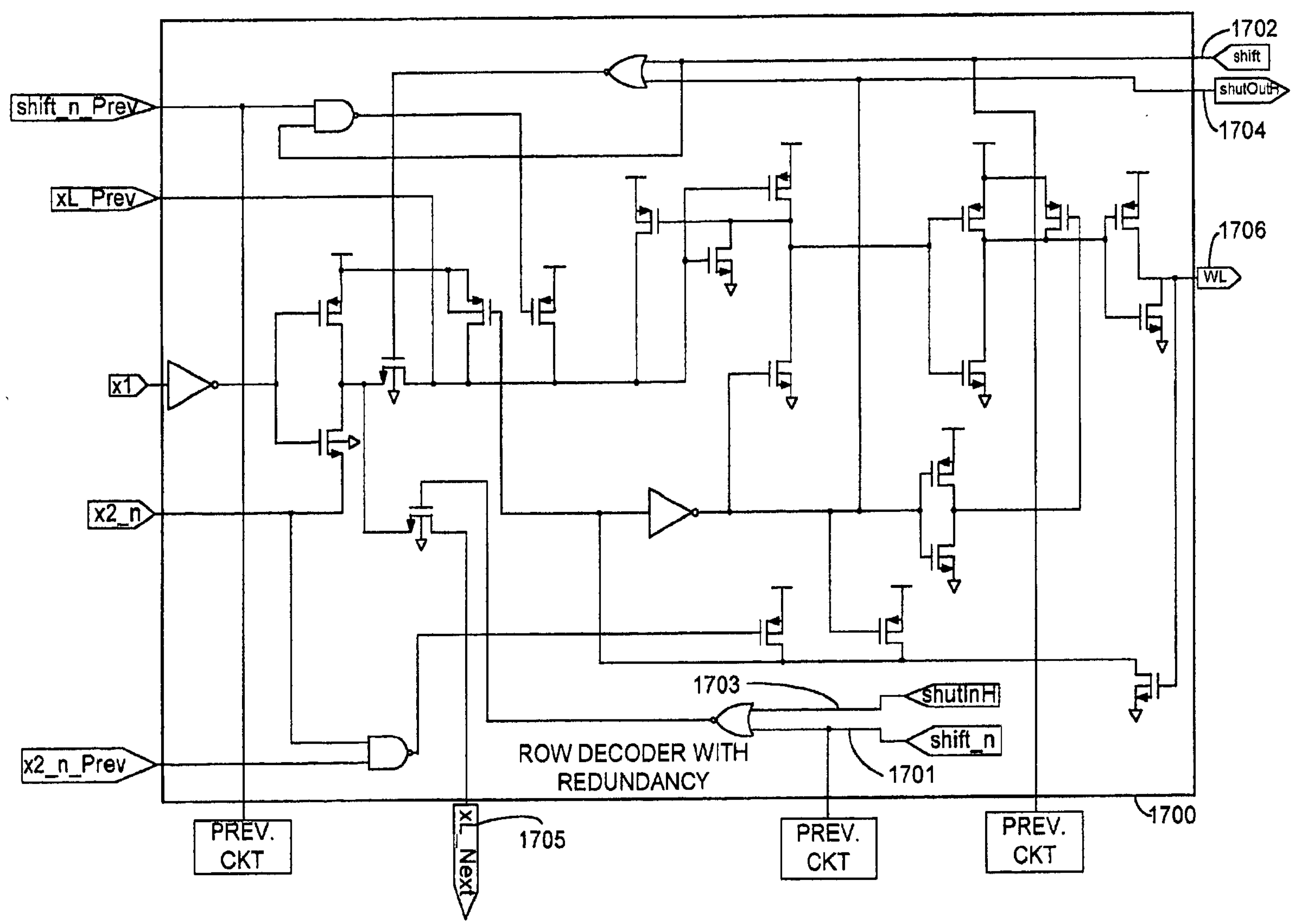
1702
shift
shutOutH
1704
1706
WL
shift_n_Prev
xL_Prev
x1
x2_n
x2_n_Prev
1703
shutInH
shift_n
1701
ROW DECODER WITH
REDUNDANCY
1700
PREV.
CKT
xL_Next
1705
PREV.
CKT
PREV.
CKT

FIG. 17

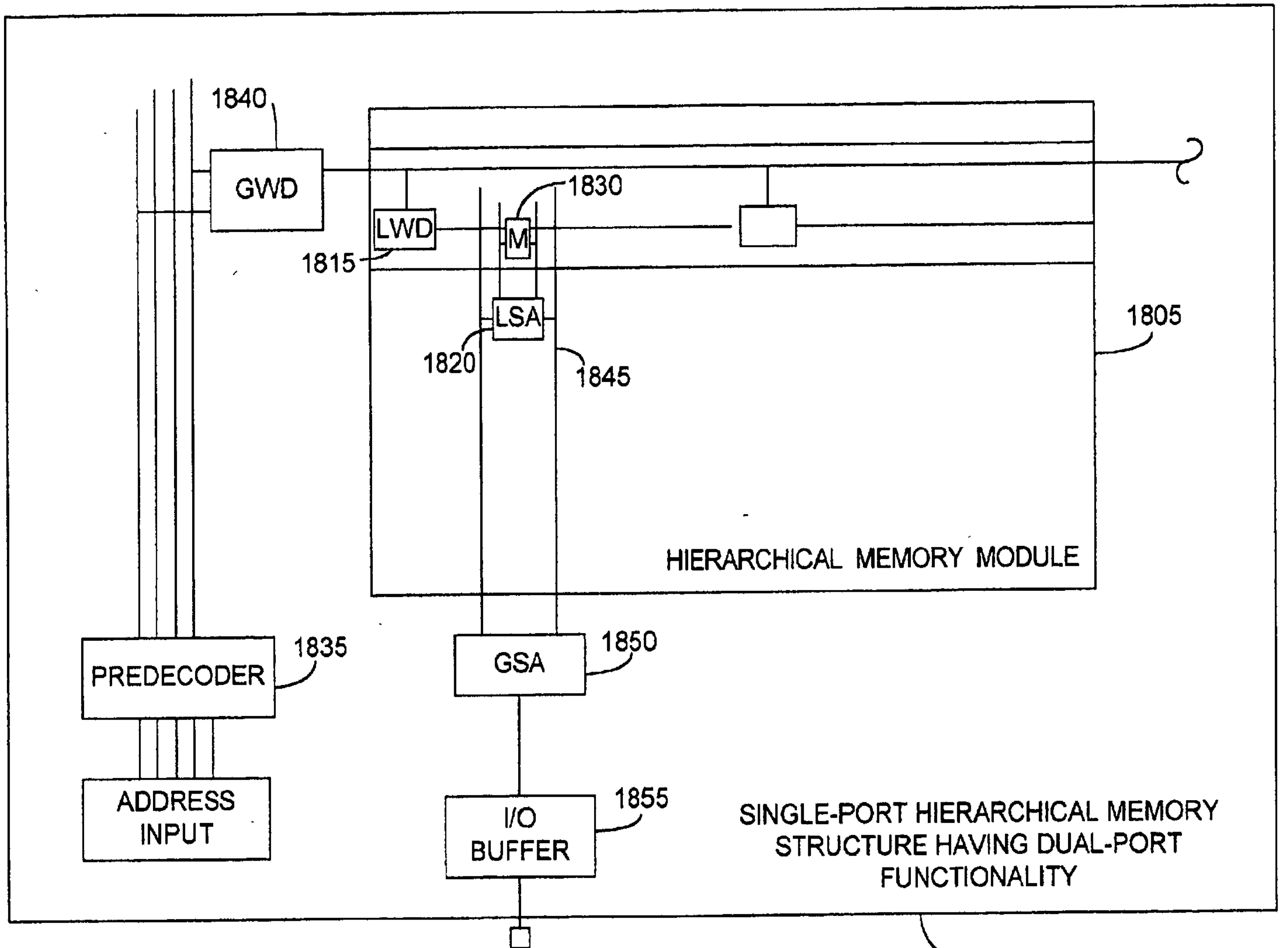
1840
GWD
LWD
1815
M
1830
LSA
1820
1845
1805
HIERARCHICAL MEMORY MODULE
PREDECODER
1835
ADDRESS INPUT
GSA
1850
I/O BUFFER
1855
SINGLE-PORT HIERARCHICAL MEMORY STRUCTURE HAVING DUAL-PORT FUNCTIONALITY
1800

FIG. 18

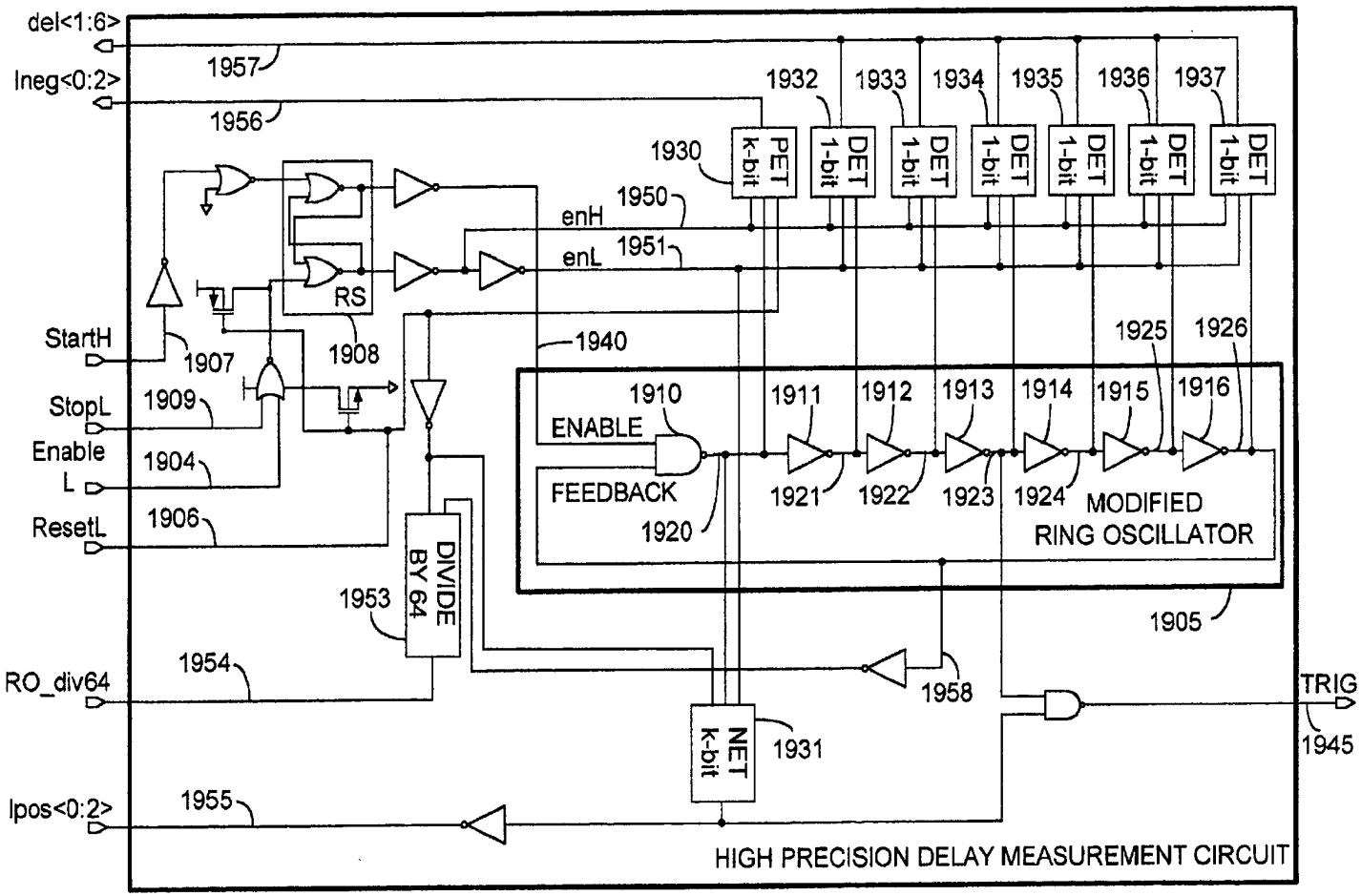
del<1:6>
Ineg<0:2>
1957
1956
1932
1933
1934
1935
1936
1937
1930
PET k-bit
DET 1-bit
1950
enH
enL
1951
RS
1908
1940
1925
1926
StartH
1907
1910
1911
1912
1913
1914
1915
1916
StopL
1909
ENABLE
Enable L
1904
FEEDBACK
1920
1921
1922
1923
1924
MODIFIED RING OSCILLATOR
ResetL
1906
DIVIDE BY 64
1953
1905
1954
RO_div64
1958
TRIG
1945
NET k-bit
1931
Ipos<0:2>
1955
HIGH PRECISION DELAY MEASUREMENT CIRCUIT

FIG. 19

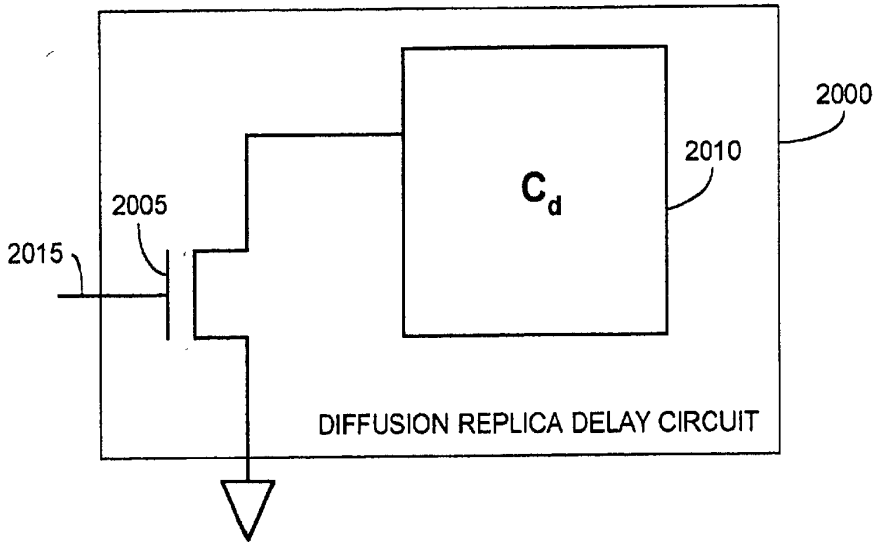

FIG. 20

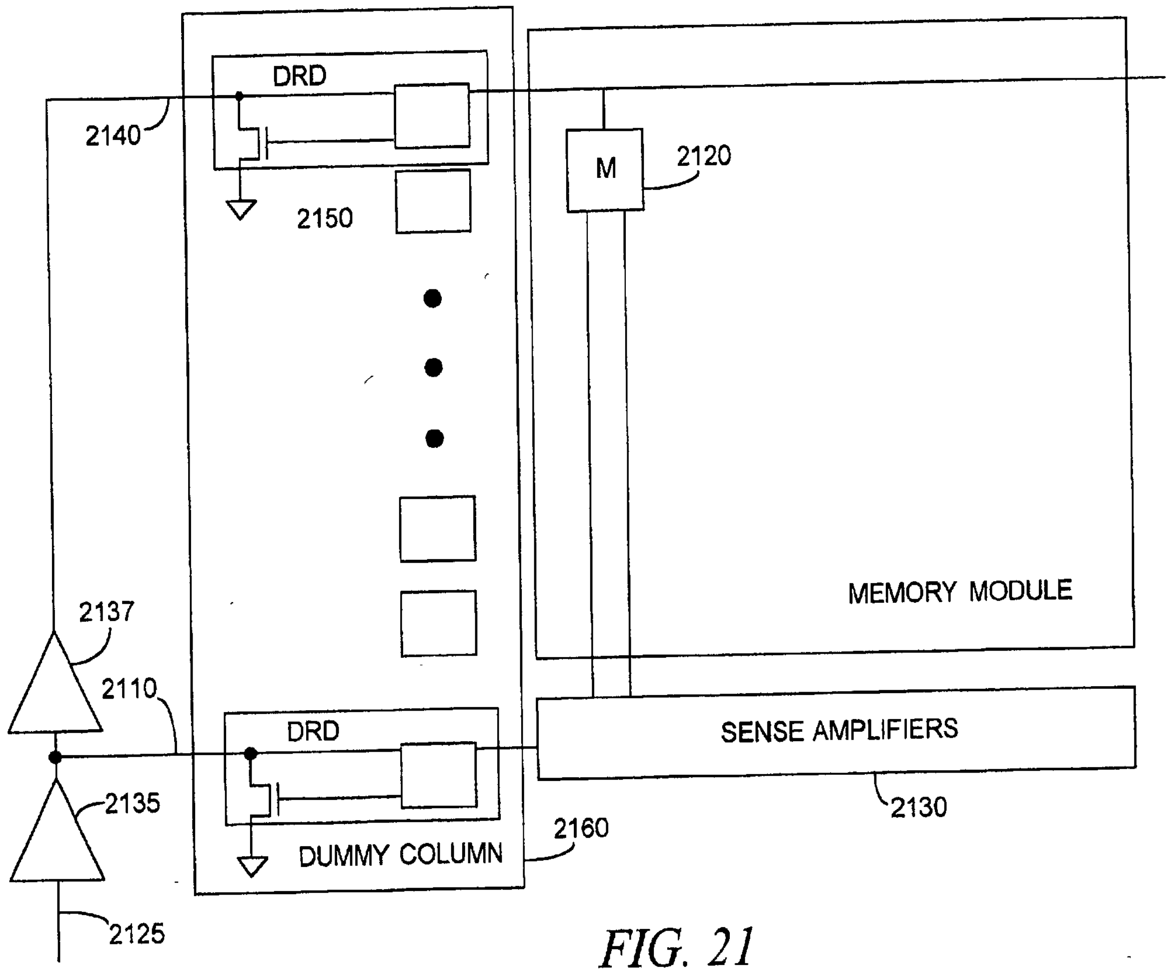
DRD
2140
2120
M
2150
MEMORY MODULE
2137
2110
DRD
SENSE AMPLIFIERS
2135
2130
2160
DUMMY COLUMN
2125

FIG. 21

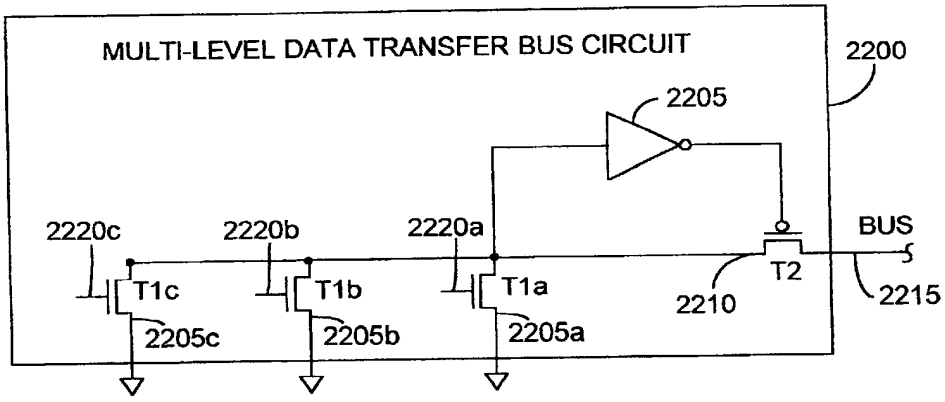

FIG. 22A

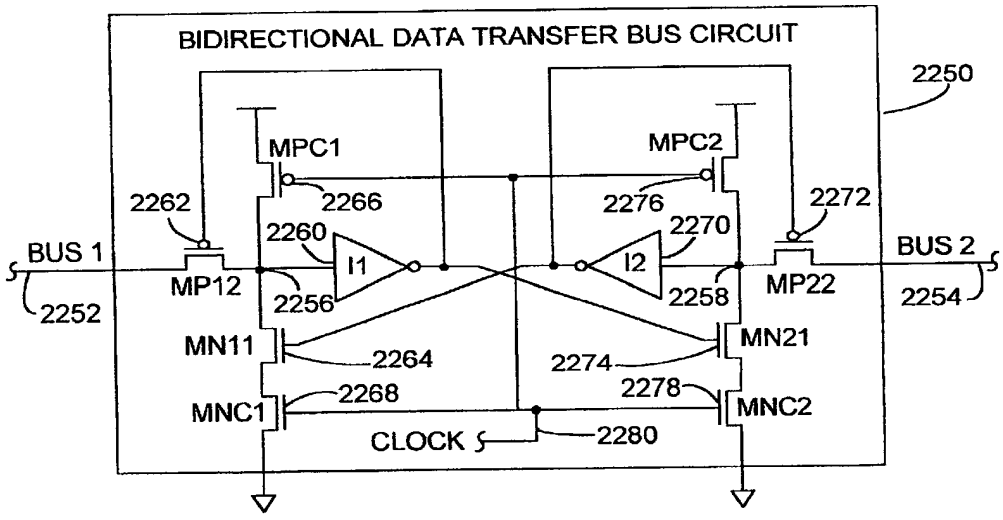

FIG. 22B